Machine Code Mappings

## Machine Code Table

|  |  |  |  |
| --- | --- | --- | --- |
| Command | OPCODE | OPERANDS | DESCRIPTION |
| IMME | 10 | rs, (32 LUT) | Load 8 bit immediate fron LUT into rs |
| BLT | 110 | Branch (64 LUT) | Branch by amt in LUT |
| BNE | 111 | Branch (64 LUT) | Branch by amt in LUT |
| ADD | 00000 | rs, rt | rs = rs + rt |
| ADDC | 00001 | rs, rt | rs = rs + rt\* (rt in secondary register table) |
| SUB | 00010 | rs, rt | rs = rs - rt |
| SUBC | 00011 | rs, rt | rs = rs - rt\* (rt in secondary register table) |
| LSL | 00100 | rs, rt | rs = rs << rt |
| LSLC | 00101 | rs, rt | rs = rs << rt\* (rt in secondary register table) |
| LSR | 00110 | rs, rt | rs = rs >> rt |
| LSRC | 00111 | rs, rt | rs = rs >> rt\* (rt in secondary register table) |
| ASR | 01000 | rs, rt | rs = rs >> rt (sIGN EXTENDED |
| NEG | 01001 | rs, rt | rs = flipped rt (0>1, 1>0) |
| AND | 01010 | rs, rt | rs = rs & rt |
| OR | 01011 | rs, rt | rs = rs | rt |
| CMP | 01110 | rs, rt | CMP = rs – rt |
| LW | 01101 | rs, rt | rs = MEM[rt] |
| SW | 01100 | rs, rt | MEM[rs] = rt |
| ALW | 0111110 | rs | rs = MEM[TEMPLOC] |
| ASW | 0111111 | rs | MEM[TEMPLOC] = rs |
| HALT | 01111000 | Error | Halts machine. Operand 0= regular exit, 1 = error flag |

## Formats

RS, LUT: OPCODE – 2 bits, RS – 2 bits, LUT – 5 bits ; Order: OPCODE LUT RS

BRANCH: OPCODE – 3 bits, LUT – 6 bits ; Order: OPCODE BRANCH\_LUT

RS, RT: OPCODE – 5 bits, RS – 2 bits, RT – 2 bits ; Order: OPCODE RT RS

RS: OPCODE – 7 bits, RS – 2 bits ; Order: OPCODE RS

HALT: OPCODE – 8 bits, Overflow Flag – 1 bit; Order: OPCODE FLAG